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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/891,885 | 06/26/2001 | Mark T. Ramsbey | F0279 | 2423 |

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| EXAMINER | |
|---|---|
| MAGEE, THOMAS J | |
| ART UNIT | PAPER NUMBER |
| 2811 | |

DATE MAILED: 12/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/891,885 | RAMSBEY ET AL. | |
| | Examiner | Art Unit | |
| | Thomas J. Magee | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Cancellations*

1. Applicant's cancellation of Claims 1 – 8 in Letter No. 9 of October 4, 2002 is acknowledged. Claims 9 – 18 are pending and still active.

### *Claim Rejections – 35 U.S.C. 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 9,10 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Fliesler et al. (US 6,238,975 B1).

Fliesler et al. disclose a non-volatile memory device (Col. 7, lines 6 – 34) having a core and a peripheral region on a substrate where one or more insulating regions for one or more ESD transistors are provided in the peripheral region with a polysilicon (gate) layer formed over the insulating layers. After patterning the ESD and other transistors spacers are formed surrounding the gate structures. (Col. 2, lines 41 – 43). Heavy doping is done in ESD transistors while also doping other transistors in the peripheral region (Col. 2, lines 1 – 12).

***Claim Rejections – 35 U.S.C. 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fliesler et al., as applied to Claims 9,10, and 15 above, and further in view of Diaz et al. ("Building –in ESD/EOS Reliability for Sub-half Micron CMOS Processes," Proc. 33rd Reliability Physics Symp., 4 – 6 April, 1995, pp.276 – 283).

Fliesler et al. disclose (Col. 2, lines 27 – 29) a heavy implant of phosphorus to a dose of of 3 x 10(^)15/cm(^)2 , but do not disclose the ion energy. In a similar application with a similar structure, Diaz et al. disclose (Table 2, page 279) that the ion energy is 65 keV. In both cases, the parameters are well within the range of values recited in the instant application. Further, it would have been obvious at the time of the invention to one of ordinary skill in the art to combine Diaz et al. with Fliesler et al. to obtain an optimum ion implant condition to deploy in the memory circuit.

6. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fliesler et al., as applied to Claims 9, 10, and 15 above, and further in view of Reisinger (6,008,081).

Fliesler et al. do not explicitly disclose that the flash memory array is a SONOS type structure, but this would have been an easy modification. SONOS cells have been present since the late 1960's, although newer dielectric layers have been utilized in recent applications. Reisinger discloses (Col. 8, lines 5 – 12) the formation of MOS transistors with multiplayer dielectrics (51,52,53) capped by a polysilicon layer (6) (See Figure 1) to produce a classical SONOS structure. Hence, it would have been obvious at the time of the invention to one of ordinary skill in the art to add Reisinger to Fliesler et al. to obtain a SONOS gate dielectric structure with improved dielectric properties in the flash memory circuit.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fliesler et al., as applied to Claims 9,10, and 15 above, in view of Reisinger, as applied to Claims 12 and 13, and further in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey, (1993) pp. 860 – 873). Fliesler et al. do not disclose the spacing of word line interconnects at 1um. However, Wilson et al. disclose (pages 871 – 873, figures) a minimal signal delay for metal spacings and widths of approximately 1 um for a number of conductive materials. Further, the amount of crosstalk and normalized noise is significantly lower at dimensions of approximately 1 um (page 865, figure 7). Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art to add Reisinger and Wilson et al. to Fliesler et al. to obtain a working memory device containing SONOS cells with word lines spaced at 1 um for enhanced performance.

8. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fliesler et al. in view of Diaz et al.

As discussed earlier, Fliesler et al. disclose the formation of a non-volatile semiconductor memory device where a core and peripheral region are established with ESD and other transistors containing one or more insulating layers formed in the peripheral region. A polysilicon layer is formed over the insulating layers and subsequent patterning done prior to formation of spacer material and etching to define edge spacers. The source and drain regions are lightly doped (Col. 1, lines 66 – 67) with phosphorus (Col.7 lines 60 – 61). Fliesler et al . do not explicitly disclose the implant energy/dose product, but Diaz et al. in a similar ESD transistor construction (Table 2, page 279) disclose for both standard (control) and LDD phosphorus implants, an implant energy in the range, 25 to 50 keV, with total doses in the range, 5 x 10(^)13/cm(^)2 to 10(^)14/cm(^)2, well within the energy-dose product recited in the instant application. With the spacers in place and masks provided over core and peripheral regions, heavy ion implants are done through an opening over the peripheral region (Col. 7, lines 17 – 25) into sources and drains.

Again, Fliesler et al. do not explicitly disclose the energy-dose product for the heavy implant, but do disclose a maximum dose in the range, 3 x 10(^)15 to 6 x 10(^)15/ cm(^)2 (Col. 7, lines 54 – 56). Diaz et al. disclose (Table 2) both the energy (50 to 65 keV) and the dose (4 x 10(^)14 to 10(^)15/cm(^)2 ) used in the heavy implants, both of which are well within the range recited in the instant application.

It would have been obvious at the time of the invention to one of ordinary skill in the art

et al. to produce working devices in the non-volatile memory circuit.

### *Response to Arguments*

9. Applicant's arguments with respect to claims 9 - 18 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusions*

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305**

**5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772.**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722.**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
December 18, 2002